Application No.: 10/815,709

AMENDMENTS TO THE CLAIMS:

1-14 (Cancelled)

15. (Currently Amended) A semiconductor memory device, comprising:

a first main amplifier activated in response to an active first enable signal, for amplifying data read from a first memory cell;

a first tri-state buffer, configured to receive data provided by the first main amplifier, for driving an output node of the first tri-state buffer according to the data ~~amplified by the first main amplifier~~ when the first enable signal is active[[,]] and rendering the output node in a high impedance state when the first enable signal is inactive; and

a first latch circuit for latching and outputting data of the output node of the first tri-state buffer to the outside.

16. (Currently Amended) The semiconductor memory device according to claim 15, further comprising:

a second latch circuit; and

a switch, connected between the output node of the tri-state buffer and the second latch circuit, for connecting the output node of the tri-state buffer to the second latch circuit in a test mode[[,]] and disconnecting the output node of the tri-state buffer from the second latch circuit in a normal mode.

17. (Original) The semiconductor memory device according to claim 16, wherein either the first or second latch circuit that is not used is not allowed to conduct latch operation.

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18. (Currently Amended) The semiconductor memory device according to claim 15, further comprising:

a second main amplifier, activated in response to an active second enable signal, for amplifying data read from a second memory cell;

a second tri-state buffer for driving an output node of the second tri-state buffer according to the data amplified by the second main amplifier when the second enable signal is active[[,]] and rendering the output node in a high impedance state when the second enable signal is inactive;

a second latch circuit for latching and outputting data of the output node of the second tri-state buffer to the outside; and

a switch connected between an output node of the first latch circuit and an output node of the second latch circuit, and turned ON/OFF according to a bit width of read data.

19. (Original) The semiconductor memory device according to claim 18, wherein either the first or second latch circuit that is not used is not allowed to conduct latch operation.

20. (Currently Amended) A semiconductor memory device, comprising:

an output buffer for outputting data read from a memory cell to an output terminal, wherein

the output buffer includes

a first buffer for receiving data read from the memory cell and driving the output terminal according to the data ~~read from the memory cell~~, and

a second buffer, having an active state and an inactive state, for receiving the same data as the first buffer and driving the output terminal according to the [[read]] data only in the active state, and

the first buffer drives the output terminal irrespective of the active state and the inactive state.

21. (Currently Amended) [[The]] A semiconductor memory device ~~according to claim 20~~, comprising:

an output buffer for outputting data read from a memory cell to an output terminal, wherein the output buffer includes

a first buffer for driving the output terminal according to the data read from the memory cell, and

a second buffer, having an active state and an inactive state, for driving the output terminal according to the read data in the active state; and

the second buffer is activated and inactivated according to a bit width of the data read from the memory cell.

22. (Currently Amended) The semiconductor memory device according to claim 21, wherein the second buffer is activated and inactivated according to an external signal capable of recognizing the bit width of the data read from the memory cell.

23. (Original) The semiconductor memory device according to claim 21, wherein the second buffer is activated and inactivated by using a fuse element representing the bit width of the data read from the memory cell.

24. (Currently Amended) [[The]] A semiconductor memory device ~~according to claim 20~~, ~~further~~ comprising:

an output buffer for outputting data read from a memory cell to an output terminal; and

a detector for detecting an operating frequency of the semiconductor memory device, wherein the output buffer includes

a first buffer for driving the output terminal according to the data read from the memory cell, and

a second buffer, having an active state and an inactive state, for driving the output terminal according to the read data in the active state; and

the second buffer is activated and inactivated according to the operating frequency detected by the detector.

25-29 (Cancelled)